Lab 10

Finite State Machine

ECE 380-002

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**Introduction**

In this lab, we mainly focus on the designing of two type of finite state machine (FSM) which are Moore-type and Mealy-type. These two machines will detect the input, when the inputs contain sequence of 100, the output will be 1 else the output will be 0.

**Procedure**

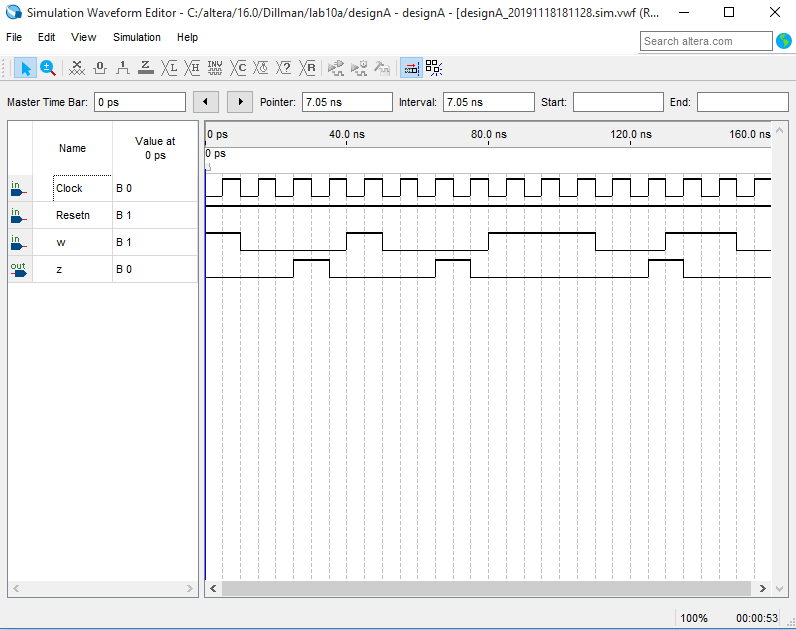
1. **Prelab**

In the prelab, we draw the bubble diagram of two machine. In the picture, diagram A is Moore-type finite state machine and diagram B is Mealy-type finite state machine.

A close up of a map

Description automatically generated

* 1. **Design A**

A screenshot of a social media post

Description automatically generatedIn the design A, we redesign the VHDL code and make some change to let the machine can detected the sequence.

* 1. **Design B**

A picture containing screenshot

Description automatically generatedA screenshot of a computer

Description automatically generatedIn the design B, we just design the same finite state machine but in the Mealy type.

1. **During the lab**
   1. **Design A**

A screenshot of a cell phone

Description automatically generatedDuring the lab, we assign the pins of the design to the DE1 board. Then we upload the design to the lab and finally we do the test manually.

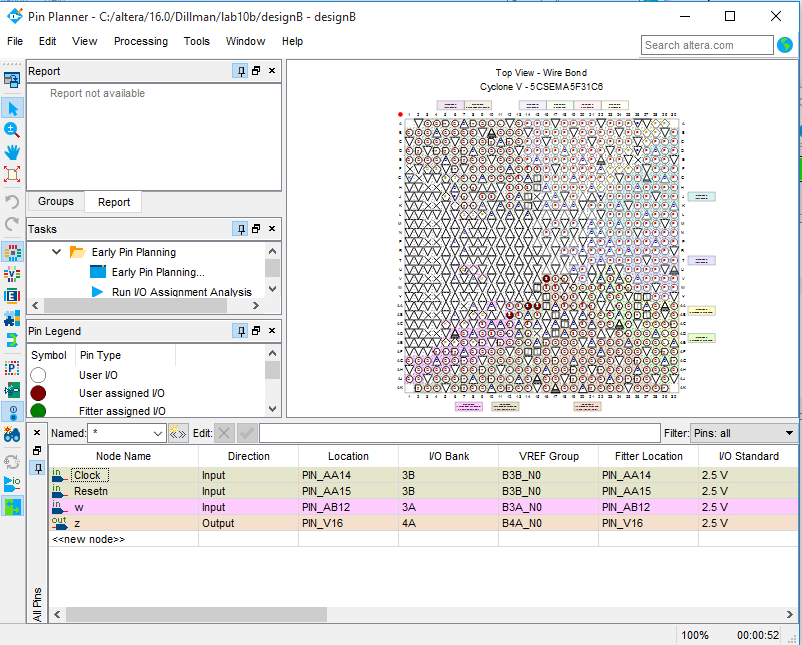
A screenshot of a cell phone

Description automatically generated

* 1. **Design B**

In the design B, we repeat the same procedure in the design A.

A screenshot of a cell phone

Description automatically generated

**Result**

In the result of the board is same as we test in the prelab.

**A screenshot of a cell phone

Description automatically generatedConclusion**